UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/966,954	11/10/1997	JOHANNES R. GERARDUS DE VRIES	6211P001	6312

7590 06/12/2007

Jordan M. Becker
Blakely, Sokoloff, Taylor & Zafman LLP
12400 Wilshire Boulevard, Seventh Floor
Los Angeles, CA 90025-1030

EXAMINER	
PETRANEK, JACOB ANDREW	
ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
06/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	08/966,954	GERARDUS DE VRIES, JOHANNES R.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *44,45,49,50 and 63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *44,45,49,50 and 63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *5/17/2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 44-45, 49-50, and 63 are pending.

2. The office acknowledges the following papers:

Specification, claims, arguments, and drawings filed on 5/17/2007.

Withdrawn objections and rejections

3. The drawing objections have been withdrawn due to amendment.

Maintained Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 44-45, 49-50, and 63 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The limitation from claims 44 and 63 "A second assembly code level which includes a plurality of instructions which are accessible to the programmer and which can explicitly reference individual outputs of any of the plurality of functional units" is not contained within the specification upon a cursory glance. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

6. Claims 45 and 49-50 are rejected due to their dependency.

New Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 44-45, 49-50, and 63 are rejected under 35 U.S.C. §103(a) as being unpatentable over Chuang (U.S. 4,766,566), in view of Labrousse et al. (U.S. 5,313,551), in view of Yokouchi (U.S. 4,958,275), in view of Blahut et al. (U.S. 4,346,437).

9. As per claim 44:

Chuang disclosed a processor comprising:

A plurality of functional units coupled to each other to execute operations defined from an instruction set of the processor (Chuang: Figure 7 elements 24, 60, 62, and 70, column 10 lines 18-41), the plurality of functional units including an arithmetic logic unit (ALU) and a multiplier (Chuang: Figure 7 elements 24, 60, 62, and 70, column 10 lines 18-41), the instruction set having a hierarchy of instruction levels, each of which can be used by a programmer to define instructions for the processor, the hierarchy of instruction levels including:

A RISC/CISC assembly code level (Chuang: Figure 7, column 5 lines 3-20)(The processor of figure 7 executes RISC instructions.), and

Chuang failed to teach a second assembly code level which includes a plurality of instructions which are accessible to the programmer and which can explicitly reference individual outputs of any of the plurality of functional units.

However, Labrousse disclosed a second assembly code level which includes a plurality of instructions which are accessible to the programmer and which can explicitly reference individual outputs of any of the plurality of functional units (Labrousse: Column 13 lines 35-42 and column 14 lines 17-22)(The instructions that contain bypass encoding signals are available to the programmer and are implemented into the instructions upon being compiled. Labrousse disclosed instructions that can be encoded with a bypass signal that can be used to bypass register reads without having a make a comparison between addresses for instructions.).

The advantage of encoding bypass signals within an instruction is that it will save the time needed to make comparisons between source registers between instructions and it will save space on the processor, which will lower costs (Labrousse: Column 2 lines 56-62). Allowing for bypass in the instruction will also result in the register value being available sooner to the instruction needing it, which may increase performance if the register access is in the critical path (Labrousse: Column 1 lines 49-64). The advantages of saving processor space and power, as well as increased performance would have motivated one of ordinary skill in the art to implement directly encoding bypass signals into instructions to execute. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement encoding bypass signals into instructions for the advantages of increased performance and decreased costs.

Chuang and Labrousse failed to teach a vector processing assembly code level, using which an individual instruction can be automatically repeated a programmable number of times on different data words; and a plurality of control registers, the plurality of hierarchical instruction levels further comprising a fourth level corresponding to the control registers, using which individual instruction words executed by one or more of the functional units can be extended by bits in the control registers on a per-instruction-cycle basis.

However, Yokouchi disclosed a vector processing assembly code level, using which an individual instruction can be used to cause an operation to be automatically repeated sequentially a programmable number of times on different data words (Yokouchi: Figure 1 element 23, column 6 lines 7-19 and column 9 lines 15-67 continued to column 10 lines 1-3)(A vector operation is defined as an operation where a large number of data words are subjected to the same arithmetic operation. Element 23 is the execution unit that repeatedly executes the ADDC instruction in table 2. The number of times the ADDC instruction is repeated is set by the MOVMOD instruction in table 2. The ADDC instruction repeats the programmed number of times on different data. The claim currently doesn't require that the repeat instruction includes a count number indicating the number of repeats. However, if it did, combining the MOVMOD and ADDC instruction would be obvious to one of ordinary skill in the art for the advantage of increased performance by eliminating an instruction and reducing the program size. In addition, according to "In re Larson" (144 USPQ 347 (CCPA 1965)), to make integral doesn't give patentability over prior art.).

The advantage of a repeat instruction is that it allows for high processing speed and a high byte efficiency (Yokouchi: Column 9 lines 63-67 continued to column 10 lines 1-3). The repeat instruction over the conventional code structure shown in table 2 also is more compact, which allows for the code segment to be executed quicker and results in increased performance. One of ordinary skill in the art at the time of the invention would have been motivated by these advantages to implement a repeatable instruction onto the processor of Chuang and Labrousse. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a repeatable instruction for the advantages of increased performance.

Chuang, Labrousse, and Yokouchi failed to teach a plurality of control registers, the plurality of hierarchical instruction levels further comprising a fourth level corresponding to the control registers, using which individual instruction words executed by one or more of the functional units can be extended by bits in the control registers on a per-instruction-cycle basis.

However, Blahut disclosed a plurality of control registers, the plurality of hierarchical instruction levels further comprising a fourth level corresponding to the control registers, using which individual instruction words executed by one or more of the functional units can be extended by bits in the control registers on a per-instruction-cycle basis (Blahut: Elements 31 and 33, column 8 lines 42-62)(Elements 31 and 33 make up the plurality of control registers, with element 33 being directed towards instruction extension. The programmer is allowed to load data into a control register that allows for the extension of instructions within the processor. The extension can be

on a per instruction basis because the programmer controls when the control register is loaded and reloaded to allow for instruction extension. When element 33 is loaded, each instruction is affected on an per-instruction-cycle basis.).

The advantage of using a control register for instruction extension is that it allows for additional instructions to be executed within the processor. Many times, instruction opcodes may all be used, thus using a control register is a way that additional instructions can be added to the processor (Blahut: Column 1 lines 61-67 continued to column 2 lines 1-67). One of ordinary skill in the art would have been motivated to implement control registers for the advantage of allowing the instruction set architecture to increase, even though no more opcode values may exist. Thus, it would have been obvious to one of ordinary skill in the art to implement control registers for extending instructions for the advantage of being able to add additional functionality to the processor.

10. As per claim 45:

Chuang, Labrousse, Davies, and Blahut disclosed a processor as recited in claim 44, wherein the second assembly code level comprises a native machine language of the processor (Labrousse: Column 13 lines 35-42 and column 14 lines 17-22)(The instructions that contain bypass encoding signals are available to the programmer and are implemented into the instructions upon being compiled. Labrousse disclosed instructions that can be encoded with a bypass signal that can be used to bypass register reads without having a make a comparison between addresses for instructions. The instructions are inherently native to the processor upon the combination and can be

used by the processor.).

11. As per claim 49:

Chuang, Labrousse, Davies, and Blahut disclosed a processor as recited in claim 44, further comprising:

A plurality of dedicated output buses, one for each of the functional units (Chuang: Figure 7 element 63, column 10 lines 18-41)(Each functionality unit has an output bus to put the data on.); and

A plurality of bus registers, each coupled to store the output of only a corresponding one of the plurality of functional units and each coupled to only a corresponding one of the plurality of dedicated output buses (Chuang: Figure 7 element 68, column 10 lines 18-41)(The output registers are coupled to the functional units and the output buses. Thus having the same functionality.).

12. As per claim 50:

Chuang, Labrousse, Davies, and Blahut disclosed a processor as recited in claim 49, wherein each of the dedicated output buses is coupled to an input of at least one other of the plurality of functional units (Chuang: Figure 7 elements 17 and 56, column 10 lines 18-41)(The bus lines are coupled to the inputs of the functional units through the register file.).

13. As per claim 63:

Claim 63 essentially recites the same limitations of claims 44-45 and 49-50. Therefore, claim 63 is rejected for the same reasons as claims 44-45 and 49-50.

Response to Arguments

14. The arguments presented by Applicant in the response, received on 5/17/2007 are partially considered persuasive.

15. Applicant argues "Written description support for the limitation "a second assembly code level which includes a plurality of instructions which are accessible to the programmer and which can explicitly reference individual outputs of any of the plurality of functional units" is found particularly in paragraph 46, especially in table 1 and the notes at the end of table 1."

This argument is not found to be persuasive for the following reason. The examiner still isn't fully convinced that this limitation has support even within table 1 and the end notes. Table 1 shows instructions referencing primarily two registers, R and S. These registers are noted at the end of table 1 stating that they can be selected from a plurality of busses. However, there isn't any mention that information stating where an operand is coming from is necessarily encoded within the instructions in table 1. The examiner believes that this could also be a list of options where the register values could be bypassed from. If the applicant has further evidence that the operand sources must be encoded within the instruction itself, then the examiner would be convinced the limitation has written description support and would withdraw the rejection.

16. Applicant argues "Davies failed to teach vector processing assembly code level, using which an individual instruction can be used to cause an operation to be automatically repeated sequentially a programmable number of times on different data words."

This argument is found to be persuasive for the following reason. The examiner agrees that Davies failed to teach this limitation. However, a new ground of rejection has been given due to the amendment.

17. Applicant argues "Blahut failed to teach a plurality of control registers, the plurality of hierarchical instruction levels further comprising a fourth level corresponding to the control registers, using which individual instruction words executed by one or more of the functional units can be extended by bits in the control registers on a per-instruction-cycle basis."

This argument is not found to be persuasive for the following reason. Element 33 allows for the instructions to be extended to allow for different sized operand values. Since all of the instructions are affected by the bits within the control register, instructions executed each cycle are affected. Thus, Blahut correctly reads upon the claimed limitation. The examiner notes that a more narrowed limitation regarding the control registers would likely overcome the current rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or

patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner, Art Unit 2183

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100